

REMARKS

Claims 1, 3, 10 and 11 have been amended, claims 12 to 14 have been rewritten in independent form with the amendments to claims 10 and 11 incorporated therein and claims 21 to 29 have been added. Claims 21 to 29 are copied from U.S. Patent No. 5,831,452 and are claims 1, 2, 4, 5, 6, 7, 9, 11 and 12 respectively therefrom. Please charge any costs to Deposit Account No. 20-0668.

Claims 3 and 10 to 13 were rejected under 35 U.S.C. 112, second paragraph. These claims have been amended to overcome the rejection.

Claims 1 to 9 and 15 to 20 were rejected under 35 U.S.C. 102(e) as being anticipated by Nowak et al. (U.S. 5,381,452) and claims 10 and 11 were rejected under 35 U.S.C. 103(a) as being unpatentable over Nowak et al. in view of Ling et al. (U.S. 4,700,086). The rejections are respectfully traversed since the subject application has claimed priority under 35 U.S.C. 119(e)(1) based upon provisional application number 60/026,769, filed September 26, 1996 whereas Nowak et al. bears a filing date of February 20, 1997. Accordingly, Nowak et al. is not available as a reference.

Furthermore, as noted above, claims 1, 2, 4, 5, 6, 7, 9, 11 and 12 have been copied from Nowak et al. for purposes of having an interference declared. Claims 1, 9 and 12 of the Nowak et al. patent could serve as counts in the proposed interference.

The claims copied from Nowak et al. Patent No. 5,831,452 read on the subject disclosure as follows:

21. A dynamic logic circuit, comprising:

a precharge transistor (3) connected to a power source for precharging a node for indicating a first logic level upon receiving a precharge signal;

discharge means (5, 11) for discharging said node to indicate a second logic level; and a switch (15) for connecting said precharge signal to said precharge transistor, said switch connected to pass said precharge signal to said precharge transistor if said node has been previously discharged to said second logic state.

22. A dynamic logic circuit as recited in claim 21, further comprising:

a keeper transistor (17) connected between said power source and a gate of said precharge transistor for keeping said node at said first logic level prior to discharging with said discharging means.

23. A dynamic logic circuit as recited in claim 22 wherein a gate of said keeper transistor is connected to an output of said dynamic logic circuit (17).

24. A dynamic logic circuit as recited in claim 22, further comprising a half keeper latch comprising a transistor (19) connected between said power source and said node and having a gate connected to an output of said dynamic logic circuit.

25. A dynamic logic circuit as recited in claim 23, further comprising a full keeper latch comprising:

a first transistor (19) connected between said power source and said node and having a gate connected to an output of said dynamic logic circuit; and

a second transistor connected between said node and electrical ground, and having a gate connect to said output of said dynamic logic circuit (11, the gate of which is connected to the circuit output via transistor 3 or transistor 17).

26. A dynamic logic circuit as recited in claim 21 wherein said discharge means comprises a series of transistors for realizing a logical AND function (transistors 5 and 11 can provide an AND function).

27. a precharge circuit for a dynamic CMOS circuit, comprising:

a precharge node (A) for holding a first voltage level indicating a first logic state;

a precharge transistor (3) connected between said precharge node and a voltage source;

a keeper transistor (17) connected between a gate of said precharge transistor and said voltage source for keeping said precharge node at said first voltage level indicating said first logic state prior to discharge; and

a switching transistor (15) controlled by a feedback signal indicating a logic state of said precharge node; said switching transistor activating said precharge transistor during a stand-by cycle only if said precharge node has been previously discharged to a second voltage level indicating a second logic state.

28. A dynamic logic circuit as recited in claim 27 wherein a gate of said keeper transistor is connected to an output of said dynamic logic circuit (17).

29. A method of precharging a dynamic CMOS circuit, comprising the steps of:

precharging a node (A) to a high voltage level indicating a first logic state during a stand-by mode;

discharging said node with connected logic circuitry (5, 11) if said logic circuitry is activated during an active mode;

precharging said node during a subsequent stand-by mode if said node was discharged during said discharging step (15); and

inhibiting the precharging of said node during said subsequent stand-by mode if said node remains precharged from a previous standy mode (feedback from output to 15).

In view of the above remarks and amendments, reconsideration and further action in view  
of the above requests is respectfully requested.

Respectfully submitted,

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